Introduction to Digital Logic for Transfer Students Lecture

ECE 2061

Description / Conditions

Transcript Abbreviation:
IntDigitalLogicLec

Course Description:
Lecture-only component of ECE 2060, for transfer students. Introduction to the theory and practice of combinational and clocked sequential networks.

Course Levels:
Undegraduate (1000-5000 level)

Designation:
Elective
Required

General Education Course:
(N/A)

Cross-Listings:
(N/A)

Course Detail

Credit Hours (Minimum if “Range” selected):
2.50

Max Credit Hours:
2.50
Select if Repeatable:
Off

Maximum Repeatable Credits:
(N/A)

Total Completions Allowed:
(N/A)

Allow Multiple Enrollments in Term:
No

Course Length:
14 weeks (autumn or spring)
12 weeks (summer only)

Off Campus:
Never

Campus Location:
Columbus

Instruction Modes:
In Person (75-100% campus; 0-24% online)
Hybrid Class (25-74% campus; 25-74% online)

Prerequisites and Co-requisites:
Prereq: Math 1152 or 1161.01 or 1161.02 or 1172 or 1181H, and Physics 1250, 1250H or 1260, and CSE 1222 or 2221 or Engr 1281.01H or 1281.02H or 1222; and Engr 1182.01 or 1182.02 or 1182.03 or 1282.01H or 1282.02H or 1282.03H, or Engr 1186 and 1187. and concur: 1188 concurrent, or 1187 and 1188 and concur: 1186, or major in CIS or CIS-PRE; and CPHR 2.00 or above.

Electronically Enforced:
No

Exclusions:

Course Goals and Learning Objectives
Course Goals / Objectives:
Master the number representations used in today's digital systems and their arithmetic properties and conversion techniques
Master analyzing and synthesizing networks of combinatorial, digital logic elements
Be competent to analyze, design and synthesize digital clocked sequential circuits
Be familiar with modern computer tools for digital design, verification and simulation
Be familiar with digital circuit design methods

Check if concurrence sought:
No

Contact Hours
### Contact Hours:

<table>
<thead>
<tr>
<th>Topic</th>
<th>LEC</th>
<th>REC out-of-class</th>
<th>REC in-class</th>
<th>Weekly LAB out-of-class</th>
<th>Weekly LAB in-class</th>
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<tbody>
<tr>
<td>Number systems and conversion</td>
<td>3.0</td>
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<tr>
<td>Boolean algebra</td>
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<td>Karnaugh maps</td>
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<tr>
<td>Multi-level gate circuits</td>
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<tr>
<td>Multiplexers, decoders and PLDs</td>
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<td>0.0</td>
<td>0</td>
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<tr>
<td>Latches and flip-flops</td>
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<td>0.0</td>
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<tr>
<td>Registers and counters</td>
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<tr>
<td>Timing (delays, timing diagrams)</td>
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<tr>
<td>Analysis of clocked sequential circuits</td>
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<tr>
<td>Design of clocked sequential circuits</td>
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<td>Finite state machines, flow diagrams, mapping to flip-flop circuits with logic gates.</td>
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### Grading and Texts

#### Grading Plan:

Letter Grade

#### Course Components:

Lecture
Grade Roster Component:
Lecture

Credit by Exam (EM):
No

Grades Breakdown:

<table>
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<tr>
<th>Aspect</th>
<th>Percent</th>
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<tbody>
<tr>
<td>Homework</td>
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<tr>
<td>Midterm Exam 1</td>
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<tr>
<td>Midterm Exam 2</td>
<td>25%</td>
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<td>Final Exam</td>
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Representative Textbooks and Other Course Materials:

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<tr>
<th>Title</th>
<th>Author</th>
<th>Year</th>
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<tbody>
<tr>
<td>Fundamentals of Logic Design</td>
<td>Roth, Jr. and Kinney</td>
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**ABET Student Learning Outcomes**

**ABET-CAC Criterion 3 Outcomes:**
(N/A)

**ABET-ETEC Criterion 3 Outcomes:**
(N/A)

**ABET-EAC Criterion 3 Outcomes:**
(N/A)

**Embedded Literacies (UG courses only)**

Embedded Literacies Info:

**Attachments / Additional Notes or Comments**
Attachments:
(N/A)

Additional Notes or Comments:
(N/A)