THE OHIO STATE UNIVERSITY
COLLEGE OF ENGINEERING

High Speed Interface Circuits and Systems Design

ECE 7023

Credit Hours:
3.00 - 3.00

Course Levels:
Graduate (5000-8000 level)

Course Components:
Lecture

Course Description:
Analysis and design of link architectures and circuits for wireline communication systems. Emphasis on design intuition, link budgeting and power/performance trade-offs in implementation of data links in advanced CMOS process. Topics include channel characterization, noise analysis, equalization, transmitter and receiver circuits, signaling schemes, clocking, synchronization and timing recovery

Prerequisites and Co-requisites:
Prereq or concur: 5020 and 5021, or permission of instructor.

Course Goals / Objectives:
- Learn fundamentals of high-speed data link design
- Learn system architecture using modeling tools
- Understand the challenges of designing high-speed wireline circuits through a design project using advanced CMOS process.
- Be exposed to several link standards, including USB-Type C, Thunderbolt, PCIe and DDR.

Course Topics:

- Basic high-speed data link concepts
- Channel characterization
- Performance metrics, link budget and trade-offs
- Equalization
- Signaling schemes
- Transmitter circuits
- Receiver circuits
- Clocking, synchronization and timing recovery
- Power and clock distribution
- Project presentations

Designation:

Elective