THE OHIO STATE UNIVERSITY
COLLEGE OF ENGINEERING

Advanced Hardware Architecture Design Techniques

ECE 5560

Credit Hours:
3.00

Course Levels:
Undergraduate (1000-5000 level)
Graduate (5000-8000 level)

Course Components:
Lecture

Course Description:
This course introduces highly-practical methodologies and techniques that can be broadly used to improve the efficiency and achieve speed-area-power tradeoffs in the design of application-specific hardware implementation architectures for various algorithms. Efficient implementation architectures of commonly used arithmetic and digital signal processing functional blocks will also be discussed.

Prerequisites and Co-requisites:
Prereq: 2050, and prereq or concur: 3561 or 3050; or Grad standing in Engr; or permission of instructor.

Course Goals / Objectives:
- Students are exposed to advanced definitions and concepts relevant to the design of digital logic architectures.
- Students become familiar with hardware architecture design methodologies for trading off speed, silicon area, and power consumption.
- Students become competent in the design of efficient architectures for commonly used arithmetic and digital signal processing functional blocks.

Course Topics:

- Characteristics and representations of signal processing programs
- Iteration bound
- Pipelining and parallel processing
- Retiming
- Unfolding
- Folding
- Fast Convolution
- Algorithmic strength reduction in filters and transformations
- Pipelined and parallel recursive filters
- Bit-level arithmetic architecture
- Redundant Arithmetic
- Numerical strength reduction
- Various implementation topics

Designation:

Elective