THE OHIO STATE UNIVERSITY
COLLEGE OF ENGINEERING

HDL Design and Verification

ECE 5462

Credit Hours:
3.00 - 3.00

Course Levels:
Undergraduate (1000-5000 level)
Graduate (5000-8000 level)

Course Components:
Lecture

Course Description:
The detailed design and verification of major components of a computer architecture using a standard hardware description language (HDL).

Prerequisites and Co-requisites:
Prereq: 5362, or 561 and 662, or CSE 675.01 or equiv, or Grad standing in Engineering.

Course Goals / Objectives:
- Introduce design of major components of computer architecture
- Introduce basic concepts of hardware description languages (HDL)
- Learn to use VHDL to specify, design, and model digital hardware components
- Learn functional verification and implement a verification plan on HDL designs. Verification of a complex component and a system of several components is done
- Learn to use HDL computer aided design tools

Course Topics:

- Advanced logic design techniques, computer architecture
- Basic of a Hardware Description Language
- Modeling of basic digital hardware
- Modeling of complex digital hardware
- Verification approaches, testing of designs, verification tools, simulators
- The verification plan, levels of verification and verification strategies
- Architecting testbenches, stimulus and response, self-checking testbenches
- PSL and assertion based verification

Designation:

Elective