THE OHIO STATE UNIVERSITY
COLLEGE OF ENGINEERING

# Introduction to Digital Logic for Transfer Students Lecture

## ECE 2061

**Credit Hours:**
2.50 - 2.50

**Course Levels:**
Undergraduate (1000-5000 level)

**Course Components:**
Lecture

**Course Description:**
Lecture-only component of ECE 2060, for transfer students. Introduction to the theory and practice of combinational and clocked sequential networks.

**Prerequisites and Co-requisites:**
Prereq: Math 1152 or 1161.01 or 1161.02 or 1172 or 1181H, and Physics 1250, 1250H or 1260, and CSE 1222 or 2221 or Engr 1281.01H or 1281.02H or 1222; and Engr 1182.01 or 1182.02 or 1182.03 or 1282.01H or 1282.02H or 1282.03H, or Engr 1186 and 1187. and concur: 1188 concurrent, or 1187 and 1188 and concur: 1186, or major in CIS or CIS-PRE; and CPHR 2.00 or above.

**Course Goals / Objectives:**
- Master the number representations used in today's digital systems and their arithmetic properties and conversion techniques
- Master analyzing and synthesizing networks of combinatorial, digital logic elements
- Be competent to analyze, design and synthesize digital clocked sequential circuits
- Be familiar with modern computer tools for digital design, verification and simulation
- Be familiar with digital circuit design methods

**Course Topics:**

- Number systems and conversion
- Boolean algebra
- Karnaugh maps
- Multi-level gate circuits
- Multiplexers, decoders and PLDs
- Latches and flip-flops
- Registers and counters
- Timing (delays, timing diagrams)
- Analysis of clocked sequential circuits (general models for sequential circuits, timing charts, state tables, graphs)
- Design of clocked sequential circuits
- Finite state machines, flow diagrams, mapping to flip-flop circuits with logic gates.

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**Designation:**
Elective
Required