THE OHIO STATE UNIVERSITY
COLLEGE OF ENGINEERING

Advanced Computer Architecture

CSE 6422

Credit Hours:
3.00 - 3.00

Course Levels:
Graduate (5000-8000 level)

Course Components:
Lecture

Course Description:
Fundamental design issues in parallel architectures, design of scalable shared memory and distributed memory systems, interconnection networks (on-chip and off-chip), multi-core architectures, accelerators, embedded systems, and exascale systems.

Prerequisites and Co-requisites:
Prereq: 6421 (775) and 6441 (721).

Course Goals / Objectives:
- Master the principles of advanced computer architecture
- Master the implications of different ways of using hardware parallelism (processors, interconnection networks and accelerators)
- Master the architectural design issues in shared memory, distributed-memory, distributed shared memory, and petascale/exascale systems
- Master the design principles of interconnection networks
- Be familiar with the architectural designs of past and present (state-of-the-art) computer systems
- Be familiar with analyzing and solving architectural design problems
- Be exposed to the future trends in parallel computer architectures

Course Topics:

- Design issues of Parallel Architectures
- Interconnection Network Design Principles (Classification of interconnection networks, basic switching techniques, virtual channels)
- Design Principles (Cont'd): Deadlock, Livelock, and Starvation; Routing Algorithms for direct, indirect, and switch-based networks; System support, hardware implementations, and software implementations for collective communication
- Latest Multi-core Architectures
- On-Chip Interconnect Architectures
- Design of Shared-Memory Multiprocessors (Cache Coherence, Memory Consistency, Snooping Protocols, Protocol Design Tradeoffs, Synchronization, and Implications on Software)
- Snoop-based Multiprocessor (Symmetric Multiprocessor) Design (Single-level cache with an atomic bus, multi-level cache hierarchies and split-transaction bus.)
- Acclerator Architectures
- Issues in Designing Scalable Systems (DSM Systems with Directory-based Cache Coherence, Software DSM Systems, and Scalable Non Cache Coherent Systems Supporting PGAS Models)
- Architectural Issues in Designing Power-Aware and Embedded Computing Systems
- Overview of Current Multi-Petaflop Systems and Architecture for Emerging Exascale Systems

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Designation:

Elective